Eight Channel Swift Digitizer for IRM

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This note describes a multi channel digitizer interface board for use in an Internet Rack Monitor. It is intended to collect relatively fast data for use as snapshot waveforms of various accelerator parameters that are available as analog signals. A diagram of this interface board is shown in Figure 1.

Overview

Characteristics of the digitizer board are:

Number of Channels:	8
Max digitize rate:	800 kHz
Digitizer resolution:	12 bits
Input Voltage Range:	±10V
Memory per channel:	4 k samples
Input impedance	>10 MΩ or 50 Ω, Jumper selectable
Digitize rates (kHz):	800, 400, 200, 100, 50, 25, 12.5, 6.25, External
Cycle Start:	CPU initiated External trigger pulse Delayed trigger from TCLK event

This interface board contains eight identical channels. Each consists of a Burr Brown ADS7810 800 kHz digitizer followed by two Cypress CY7C433A 4 kByte FIFO memory chips. These provide a memory depth that allows a 10μs sampled data to be collected during the entire Booster beam cycle. Pin compatible 1- and 2-kByte FIFO parts are also available. The 800 kHz digitize rate of the ADS7810 is fast enough to acquire turn-by-turn data from the Booster at extraction time. Because the input impedance of the digitizer is only 3 kΩ, a Burr Brown BUF634 unity gain buffer is included as the input stage for each channel. Also, a jumper is included to terminate the input signal in a 50 Ω resistor.

Data collected by this module is thought of as snapshot data; the device is armed by the computer, triggered to begin data collection, and then latched off when the FIFO memories are filled. FIFO data appears as eight words of data in the I/O space of the controlling IP module. An additional register is used to read out the FIFO *empty flag* and *full flag* status for each channel. Figure 2 shows the memory map of the Swift Digitizer system including the assignment of the control register bits.

The Swift A-D interface board is controlled by the same IP module used for the analog I/O of the IRM, except the Actel gate array is modified to control the faster digitizers. Figure 3 gives the pinout of the interface connector. Figure 4 shows the Actel FPGA chip used to control the swift digitizer board.

The system is armed by the host CPU to enable it to start digitizing when the selected trigger is detected. Trigger sources include a software trigger by the host cpu, an external trigger pulse, or an internally generated trigger that is delayed from a selected event on the TCLK. The event register and the delay logic are contained in the Actel gate array on the IP module.

Details of the Swift A-D Operation and Registers

Addressing
The base address of the Swift A-D is determined by the host computer or IP carrier board. The next $30 bytes of I/O memory are used for control, status and readout of digitizer data.

Base + $00...Base + $0F: Eight words of FIFO data from the eight digitizer channels. Successive digitized values are read by repetitively reading the same memory location. The data values are twos complement, left justified.

Base + $10: *Full* status for the eight digitizer channels. A binary "0" indicates the FIFO has no space available to accept data.

Base + $11: *Empty* status for the eight digitizer channels. A binary "0" indicates the FIFO contains no valid data to be read.

Base + $20: A write operation to this location will *Start* an acquisition sequence. Any *Start* will issue a master clear to all the FIFOs.

Base + $21: A write operation to this location will *Stop* an acquisition sequence that is in progress. If the sequence has already stopped, the write to $21 will have no effect.

Base + $22: A write operation to this location arms all FIFOs. The control circuitry is then ready to accept a trigger from the selected trigger source, to initiate a sequence.

Base + $23: A write operation to this location performs a master reset to all FIFOs.

Base + $26: The upper five bits are used read the Full Status, Empty Status, Busy Status, and Armed Status in bits 7,6,5,and 4, respectively. Bit 4 is unused and reads as a "0". The low three bits of byte $26 control the digitize rate as shown in Figure 2b.

Base + 27: A-D control/status register; Bit 7 = 1 enables the A-Ds. When Bit 7 is high and the digitizer is armed, a digitize sequence may be initiated by the selected trigger; Bit 6 = 1 sets the system into the "Auto Trigger" mode, which means that the digitizer need not be in an armed condition for the trigger to initiate a digitize sequence;Bit 5 =1 enables IP interrupt, INT1, to be generated when Busy returns to zero.; Bit4=1 enables the output of the delay timer to assert IP interrupt, INT0. Bit 3 = 0 allows the digitize sequence to continue till the FIFOs are full. If Bit 3= 1, a second *Start* trigger will stop the digitize sequence. This feature can be used to prevent data from two or more Booster cycles to be collected during a single sequence. Bit 2 = 0 causes the internally generated digitize rate to be used. Bit 2 = 1 allows an external rep rate pulse train to clock the A-Ds. This mode can be used to collect synchronous turn-by-turn data from circular machines such as the Booster or Main Ring. Bits 0 and 1 select the sequence trigger source. Bit 1,0 = 0 selects the the delay timer output as the start trigger, Bit 1,0 = 1 selects the external trigger as the sequence start. Bits 1,0 = 2 or 3 selects the CPU Trigger mode, a write to location Base + $20.
Base + $28, $29: Delay value word for the delay timer. Delay increments are 100 ns or 1 μs depending on value of Bit 6 of the *Timer Control Register*.

Base + $2D: Selected Clock Event Register. This register holds the value of the clock event to be used to start the delay timer.

Base + $2F: Timer Control Register. Bit 7 enables the timer output. Bit 6 prescales the 10 MHz clock rate by ten. The value of the delay is then in units of microseconds. Bit 0 = 0 causes the timer to trigger on all Booster resets. Bit 0 = 1 triggers the delay timer with the arrival of the selected TCLK event.

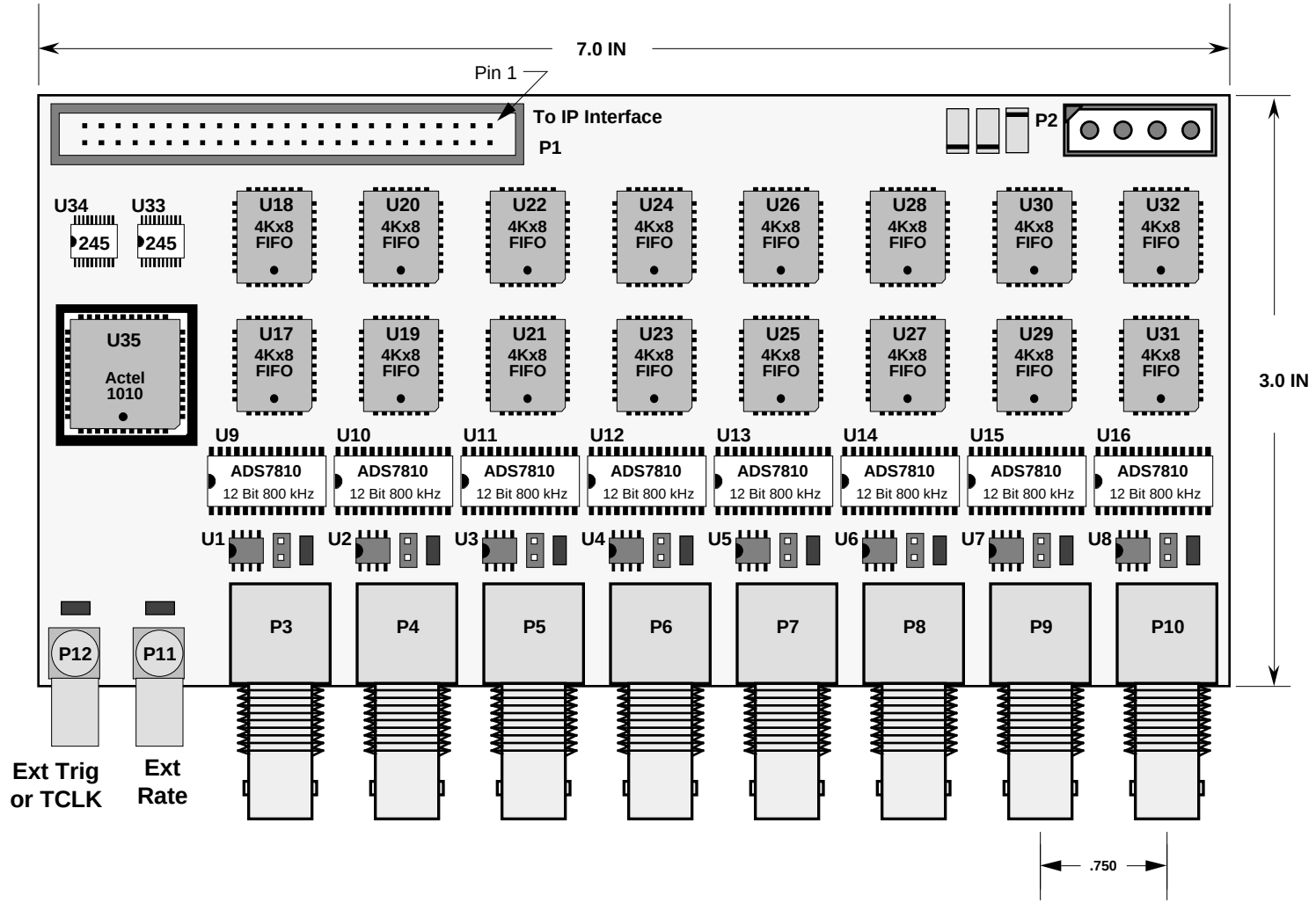

Figure 1. IRM Swift Analog Interface Board

m/s m/k 040695

Address				
Base + $00	Chan0 FIFO	Chan1 FIFO	Chan2 FIFO	Chan3 FIFO
Base + $08	Chan4 FiFo	Chan5 FIFO	Chan6 FIFO	Chan7 FIFO
Base + $10		–	–	–
Base + $18	–	-	–	–
Base + $20	Start • Stop	Arm • FIFO Clear	RamAddress	tat/Rate Sel • AD Ctrl Re
Base + $28	Timer Delay	IntV1 – IntV0	– • Sel CLK Event	– • Tmr Ctrl R
Base + $30	–	–	–	–
Base + $38	–	–	–	–

Figure 2a. Memory Map for Swift A-D FPGA

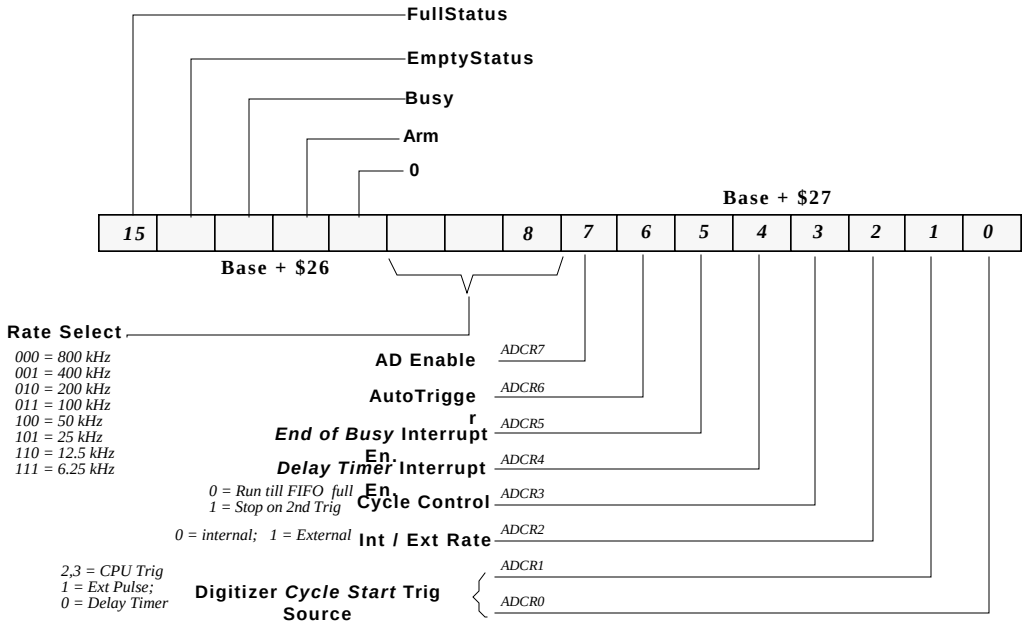

Figure 2b. Swift A-D Control/Status Register

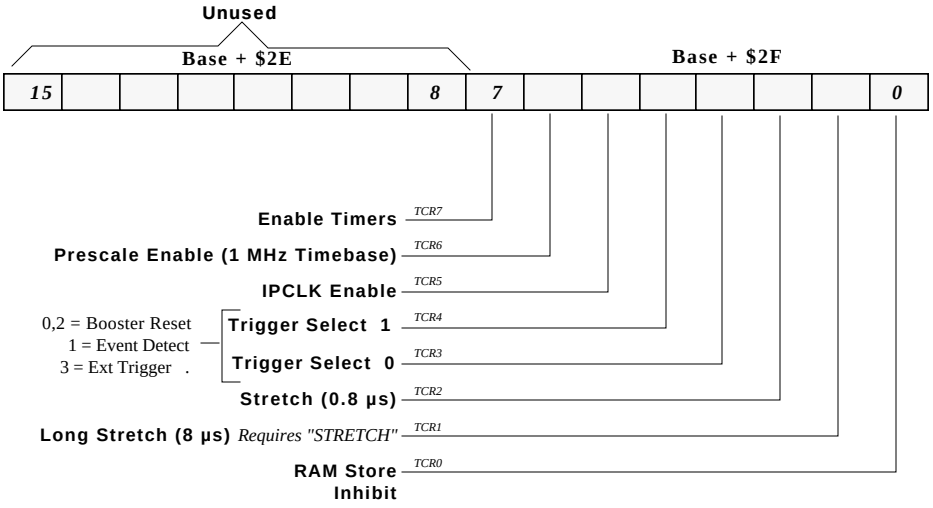

Figure 2c. Swift A-D Timer Control Register

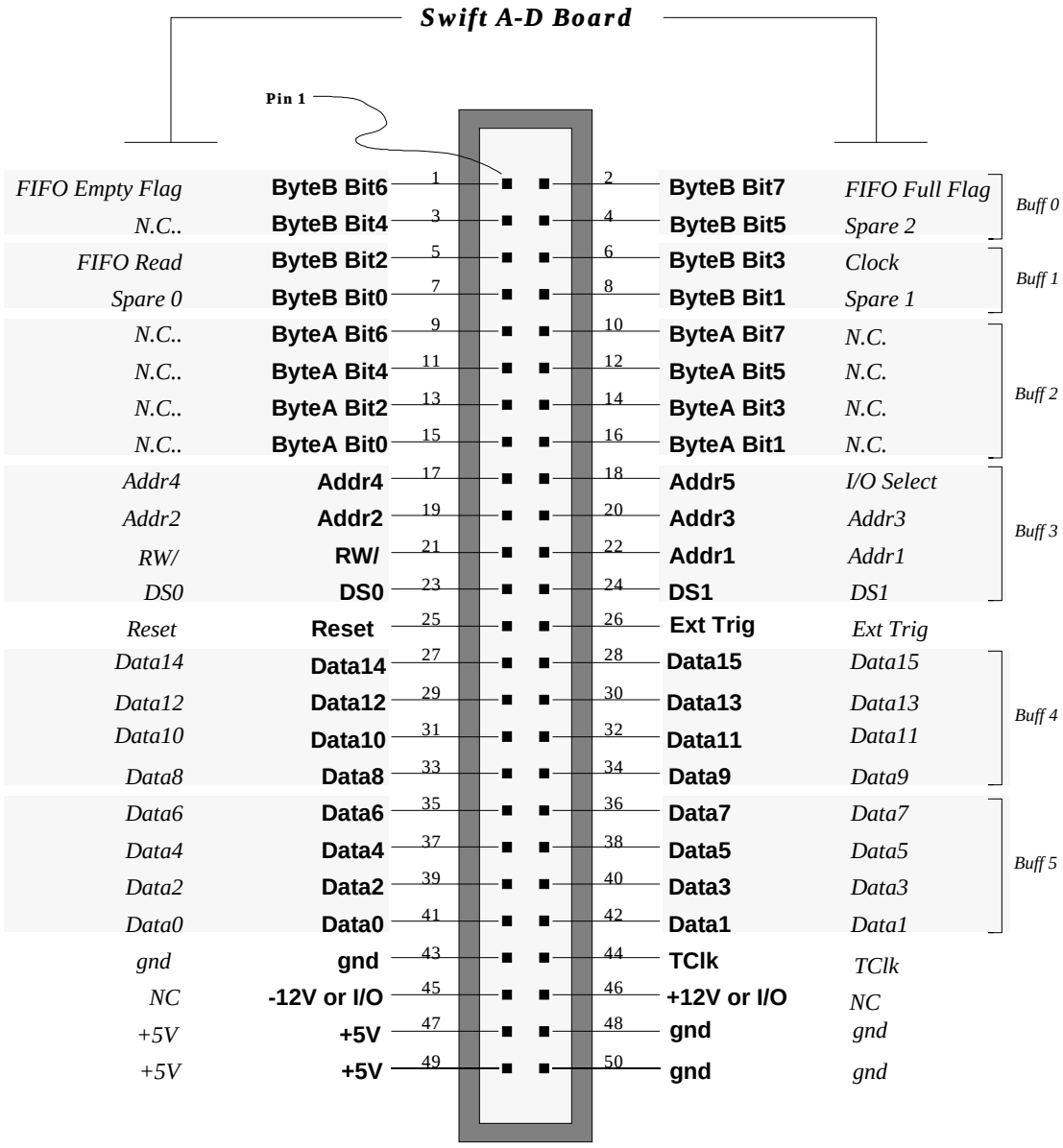

Figure 3. Swift A-D Interface Connector Pinout

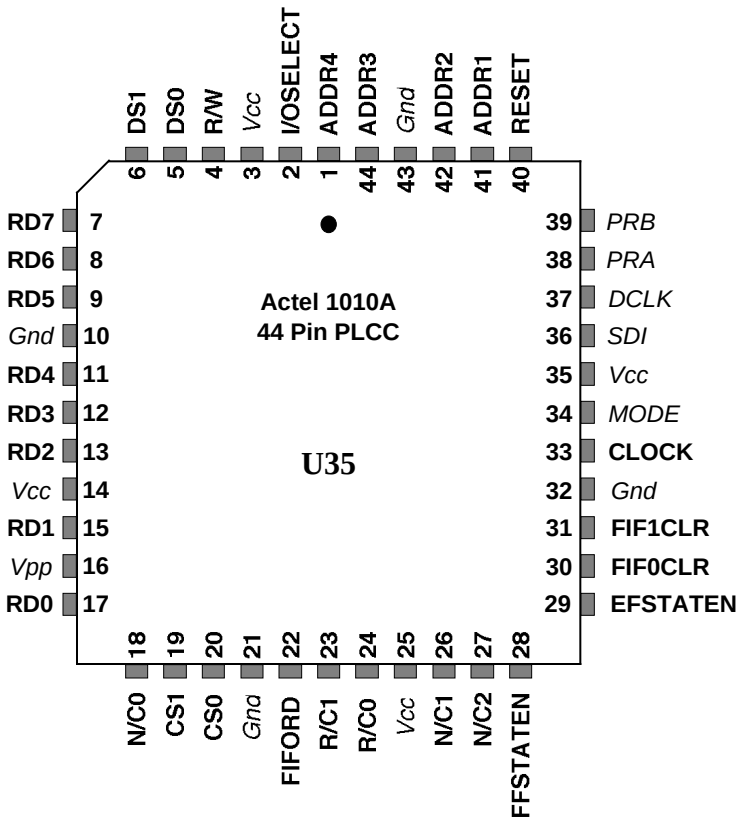

Figure 4. IRM Swift Analog Outboard FPGA